Attorney's Docket No.: 10417-057002 / F51-160880M/SW

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Shuichi Kikuchi et al.
Serial No. : 10/651,855
Filed : August 29, 2003
Title : SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING IT

Art Unit : 2813
Examiner : Thanh Nguyen

**Mail Stop Amendment**
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

REPLY TO ACTION OF SEPTEMBER 27, 2005

In reply to the Office Action of September 27, 2005, Applicants submit the following remarks.

Claims 1-3 were rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,932,897 (Kawaguchi et al.). Applicants respectfully disagree with that rejection.

Claim 1 recites a drain region, a drift region and an impurities layer. The drain region is in direct contact with the drift region and the impurities layer is adjacent to the drain region. The impurities layer is more highly doped than the drift region.

An example of those features is disclosed in FIG. 7 where drain region 12 is in direct contact with drift region 4 and impurities layer 7A is adjacent to the drain region 12. The illustrated impurities layer 7A (FP) is more highly doped than the drift region 4 (LP). In certain implementations, the features recited in claim 1 can improve a transistor's on-state resistance without adversely affecting its withstand voltage. The Kawaguchi et al. patent does not disclose or suggest those features.

CERTIFICATE OF MAILING BY FIRST CLASS MAIL

I hereby certify under 37 CFR §1.8(a) that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage on the date indicated below and is addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

December 23, 2005
Date of Deposit

Signature

Rose Syracuse
Typed or Printed Name of Person Signing Certificate